WHAT IS CLAIMED IS:

1. An ECC based method within an integrated circuit memory for self-repair of a failed memory element therein, comprising:

automatically recording locations of memory failures within said integrated circuit by processing, within said integrated circuit, data and check bits retrieved from addressed memory locations;

using first logic circuits within said integrated circuit to automatically identify failure patterns based on said locations; and

using at least second logic circuits within said integrated circuit to automatically replace a failed memory element with a redundancy element based on at least one said identified failure pattern,

whereby said failed memory element within said integrated circuit is identified and repaired automatically by circuitry within said integrated circuit.

2. The method of Claim 1 wherein said integrated circuit memory is of the type selected from dynamic random access memory (DRAM), static random access memory (SRAM), and electrically erasable programmable read only memory (EEPROM) including flash memory.

3. The method of Claim 1 wherein said failed memory element is replaced with a redundancy element selected from the group consisting of at least row redundancy element and column

redundancy element.

4. The method of Claim 1 wherein said failed memory element is replaced with a redundancy element by electrically alterable circuit connections.

5. The method of Claim 4 wherein said electrically alterable circuit connections include at least one selected from the group consisting of electronic fuse and electronic anti-fuse.

6. The method of Claim 1 wherein said memory failures are automatically recorded, said failure patterns automatically identified, and said failed memory element is automatically replaced while said integrated circuit is in a normal operational mode.

7. The method of Claim 6 wherein said memory asserts a busy signal during the time that said memory is unavailable for access during which at least one operation is being performed from the group consisting of: identifying said failure patterns and replacing said failed memory element.

8. The method of Claim 1 wherein said locations are automatically recorded while said integrated circuit is in a normal operational mode and wherein said failed memory element is automatically replaced only during a non-normal operational mode of said integrated circuit.

9. The method of Claim 8 wherein said non-normal operational mode is of a type selected from

power-up mode or power-down mode.

10. The method of Claim 2 wherein said integrated circuit memory is incorporated within an integrated circuit having a microprocessor.

11. The method of Claim 10 wherein said integrated circuit memory is of the DRAM type and wherein said locations are automatically recorded while said integrated circuit is in a normal operational mode.

12. The method of Claim 11 wherein said failed memory element is automatically replaced when said integrated circuit remains installed within a product for normal use.

13. An integrated circuit including a self-repairing memory, comprising:

error correction code (ECC) logic circuits coupled to a memory to detect errors within strings of data and check bits retrieved from addressed storage locations within said memory;

a register responsive to output of said ECC logic circuits and to address information to record locations of memory failures corresponding to said errors.

means for automatically identifying failure patterns based on said locations; and

means for automatically replacing a failed memory element with a redundancy element based on at least one said identified failure pattern,

whereby said integrated circuit is adapted to identify and repair a failed memory element

within said integrated circuit.

14. The integrated circuit of Claim 13 wherein said memory is of the type selected from dynamic random access memory (DRAM), static random access memory (SRAM), and electrically erasable programmable read only memory (EEPROM) including flash memory.

15. The integrated circuit of Claim 13 wherein said means for automatically replacing a failed memory element includes electrically alterable circuit connections.

16. The integrated circuit of Claim 15 wherein said electrically alterable circuit connections include at least one selected from electronic fuse and electronic anti-fuse.

17. The integrated circuit of Claim 13 wherein said register, said means for identifying and said means for replacing all operate while said integrated circuit is in a normal operational mode.

18. The integrated circuit of Claim 17 wherein said memory includes an interface adapted to assert a busy signal when said memory is unavailable for access during which time at least one of said means for identifying and said means for replacing is operating.

19. The integrated circuit of Claim 13 wherein said register records said locations while said integrated circuit is in a normal operational mode and wherein said means for automatically

replacing said failed memory element operates only during a non-normal operational mode of said integrated circuit.

20. The integrated circuit of Claim 19 wherein said non-normal operational mode is of a type selected from power-up mode or power-down mode.

21. The integrated circuit of Claim 14 wherein said integrated circuit includes a microprocessor.

22. The integrated circuit of Claim 21 wherein said memory is of the DRAM type and wherein said register records said locations while said integrated circuit is in a normal operational mode.

23. The integrated circuit of Claim 22 wherein said means for automatically replacing said failed memory element operates when said integrated circuit remains installed within a product for normal use.

24. The integrated circuit of Claim 13 wherein said redundancy element is selected from the group consisting of at least row redundancy element and column redundancy element.